REMARKS

The following remarks are made in response to the Office Action mailed May 14, 2007. Claims 1-36 were rejected. With this Response, claims 1, 10-12, 19, 28, and 33 have been amended. Claims 3 and 21-23 have been canceled without prejudice as to the subject matter contained therein. Claims 1-2, 4-20, and 24-36 remain pending in the application and are presented for reconsideration and allowance.

Claim Rejections under 35 U.S.C. § 103

Claims 1-36 are rejected under 35 U.S.C. §103 as being unpatentable over U.S. Patent No. 6,407,941 (Aizawa) in view of U.S. Patent No. 4,288,860 (Trost).

Claim 1, as amended, recites *inter alia*:

> a buffer management circuit coupled to the processor system and configured to provide at least one signal to the processor system that indicates when the buffer is full and when the buffer is empty;
>
> wherein the processor system is configured to detect a rate of transactions received by the buffer by determining a number of times that the buffer is full and empty from the at least one signal over a time period ... .

Neither Aizawa nor Trost teach or suggest these features of claim 1.

Aizawa does not teach or suggest "a buffer management circuit coupled to the processor system and configured to provide at least one signal to the processor system that indicates when the buffer is full and when the buffer is empty" as recited in claim 1. Accordingly, Aizawa does not teach or suggest "wherein the processor system is configured to detect a rate of transactions received by the buffer by determining a number of times that the buffer is full and the buffer is empty from the at least one signal over a time period" as recited in claim 1.

Trost teaches that:

> [T]he oscillator rate is determined by OR-gates 324, 333, 337, and 329. ... [I]f the output of all four OR-gates ... are high, ... the variable rate oscillator operates at the maximum (2.5 megahertz) rate. Similarly, the output of all four OR-gates are low, ... the variable rate oscillator operates at the minimum (1.0 megahertz) rate. Col. 5, line 60 to col. 6, line 7.

Accordingly, Trost does not teach or suggest the above features of claim 1.

Applicant respectfully submits that claim 1 and claims 2 and 4-9 which depend from claim 1 patentably distinguish over the cited references for at least these reasons.

Claim 10, as amended, recites *inter alia* "wherein the memory card is configured to count a number of transactions received by the memory card from the host device during a time period ... ."

Neither Aizawa nor Trost teach or suggest these features of claim 10. Applicant respectfully submits that claim 10 and claims 11-18 which depend from claim 10 patentably distinguish over the cited references for at least these reasons.

Claim 19, as amended, recites *inter alia* "determining a first rate of transactions received by a buffer in a memory card by comparing an amount of information stored in the buffer to a threshold level ... ."

Neither Aizawa nor Trost teach or suggest these features of claim 19. Applicant respectfully submits that claim 19 and claims 20 and 24-27 which depend from claim 19 patentably distinguish over the cited references for at least these reasons.

Claim 28, as amended, recites *inter alia* "means for counting a number of the transactions received by the buffer over a time period; and means for causing the clock signal to be set at a rate associated with the number of transactions."

Neither Aizawa nor Trost teach or suggest these features of claim 28. Applicant respectfully submits that claim 28 and claims 29-32 which depend from claim 28 patentably distinguish over the cited references for at least these reasons.

Claim 33, as amended, recites *inter alia* "wherein the processor system is configured to count a number of transactions received by the buffer over a time period, wherein the processor system is configured to cause the control circuit to set a first clock signal to a first clock rate that varies in dependence on the number of transactions received by the buffer ... ."

Neither Aizawa nor Trost teach or suggest these features of claim 33. Applicant respectfully submits that claim 33 and claims 34-36 which depend from claim 33 patentably distinguish over the cited references for at least these reasons.

CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 1-2, 4-20, and 24-36 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 1-2, 4-20, and 24-36 is respectfully requested.

No fees are required under 37 C.F.R. 1.16(h)(i). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 08-2025.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Response should be directed to Wendell J. Jones at Telephone No. (408) 938-0980, Facsimile No. (650) 852-8063 or Christopher P. Kosh at Telephone No. (512) 241-2403, Facsimile No. (512) 241-2409. In addition, all correspondence should continue to be directed to the following address:

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